

### **Remarks**

The present application was filed on February 28, 2002. This Amendment is responsive to the Office Action mailed August 16, 2004 which provided an objection to the drawings and a rejection of claims 1-27. The Applicant has amended the specification and drawings in order to obviate the objection/rejection. The Applicant has furthermore amended claims 1-3, 5, 6, 13, 15, 16 and 18-22 to more particularly point out and distinctly claim that which is patentable subject matter. These amendments are proper, do not introduce new matter, are broadening of claim scope, are not narrowing in view of a prior art rejection, and place the application in proper condition for reconsideration and allowance of all pending claims.

### **Objection to Drawings**

The drawings were objected to for not explicitly referencing the data channel 230. This objection is traversed on the basis that one skilled in the art recognizes from the specification and drawings that the data channel 230 includes the interface circuit 232, the write channel 234, and the read channel 236 (see specification, page 12 lines 25-30). The interface circuit 232, write channel 234, and read channel 236 are furthermore explicitly defined in relation to FIG. 10 ( see specification, page 13 lines 1-14). Nevertheless, the Applicant has amended FIG. 10 to show reference number 230, making more explicit that which was before explicit in order to obviate the objection. Reconsideration and withdrawal of the present objection are respectfully requested.

The drawings were further objected to for not explicitly mentioning the step 308 of FIG. 11 in the specification. The Applicant has amended paragraph [0071] to make explicit that which was implicit, and has amended paragraphs [0095] and [0099] to

correct typographical errors, thereby obviating this objection. Reconsideration and withdrawal of the present objection are respectfully requested.

**Rejection Under 35 USC 102(e)**

Claims 1-27 were rejected as being anticipated by U.S. Patent No. 6,442,730 issued to Schachner ("Schachner '730"). This rejection is respectfully traversed.

**Claim 1**

Schachner '730 cannot sustain the Section 102 rejection because it does not disclose all the features of claim 1, which recites at least the following:

*an emulation circuit...which arranges the input data into an input sequence of multibit symbols each having a first selected symbol length and arranges the output data into an output sequence of multibit symbols each having the first selected length, wherein the emulation circuit determines a number of erroneous symbols in the output sequence in relation to differences between the input sequence and the output sequence....*  
(excerpt of claim 1, emphasis added)

The embodiments of the present invention as claimed in claim 1 cover a digital channel that both stores input data to a medium and subsequently retrieves output data from the medium. This claimed subject matter is supported in the specification in at least the following excerpts: "Referring now to FIG. 5, shown therein is a general block diagram of a readback circuit 135 useful in recovering the data encoded by FIG. 3." (page 9, lines 5-6); "FIG. 7 generally represents a readback circuit 165 used to recover the data encoded by FIG. 6." (page 11, lines 16-17).

Claim 1 further explicitly recites the emulation circuit arranging the input data into an input sequence and arranging the output data into an output sequence. Thus, the embodiments of the present invention as claimed in claim 1 determines the number of erroneous symbols, or predicted error rate performance, in relation to differences between

the input sequence and the output sequence.

Schachner '730 contrarily analyzes an analog input signal from the data storage medium in relation to a reference signal. The reference signal is a benchmark providing expected values; see, for example, Schachner '730 col. 14 lines 49-51: "During use the user negotiates through the appropriate menus and stores a "good" reference analog waveform 310 and then inputs an input waveform 320 to be tested."

Furthermore, Schachner '730 is inherently incapable of determining the error rate performance in accordance with embodiments of the present invention as claimed in claim 1 because it does not contemplate emulating the write channel whatsoever. See, for example: "Thus, this improved apparatus and method of the invention improve the user's ability to: Analyze PRML signals from the pre-amp through the output channel." (Schachner '730, col. 2 lines 32-33)

The Applicant expressly traverses the Examiner's following assertion in the Office Action: "Schachner teaches a reference signal is selected as an input sequence for comparing with readback (output) data to track errors...." This statement overreachingly reads the claimed comparison of the input sequence and output sequence of claim 1 onto Schachner '730's comparison of an input signal to an input reference value. See, for example, Schachner '730 claim 2 which recites "receiving a reference signal." Schachner '730 neither discloses nor suggests predicting an error rate on the comparative basis of an input sequence and a corresponding output sequence. The Examiner's construction of claim 1, forming the basis of the rejection, is erroneously too broad thereby denying the Applicant's rightful claimed subject matter.

Schachner '730 is silent regarding determining errors in relation to differences between the input sequence and the output sequence. Accordingly, the Section 102 rejection over Schachner '730 is erroneous as a matter of law because the cited reference

does not disclose all the features recited by claim 1. Reconsideration and withdrawal of the present rejection of claim 1 and the claims depending therefrom are respectfully requested.

#### Claim 15

Schachner '730 cannot sustain the Section 102 rejection because it does not disclose all the features of claim 15, which recites at least the following:

*comparing the output sequence with the input sequence to  
determine a first number of erroneous symbols in the  
output sequence.*  
(excerpt of claim 15, emphasis added)

As discussed above for claim 1, the embodiments of the present invention as claimed in claim 15 cover arranging input data into an input sequence and arranging the associated output data into an output sequence. The error performance is determined on the basis of comparing these input and output sequences.

As further discussed above for claim 1, Schachner '730 only compares two inputs and is inherently incapable of the claimed comparison because it contemplates emulating only the read channel, and not the write channel. Schachner '730 is silent regarding the claimed comparing the output sequence with the input sequence to determine a first number of erroneous symbols in the output sequence. Accordingly, the Section 102 rejection over Schachner '730 is erroneous as a matter of law because the cited reference does not disclose all the features recited by claim 15. Reconsideration and withdrawal of the present rejection of claim 15 and the claims depending therefrom are respectfully requested.

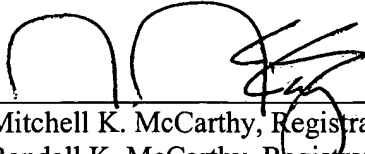
#### Conclusion

This is a complete response to the Office Action mailed August 16, 2004. The Applicant respectfully requests that the Examiner enter the above amendments,

reconsider the application and allow all of the pending claims. The Examiner is invited to contact the below signed Attorney should any questions arise concerning this response.

Respectfully submitted,

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### **Amendments to the Drawings**

The attached sheets of drawings include changes to FIGS. 7, 10 and 11. Sheet 3/7, which includes FIGS. 6 and 7, replaces the original sheet 3/7. Sheet 5/7 (FIG. 10) and sheet 6/7 (FIG. 11) replace the original sheet 5/7 and 6/7. In FIG. 7, reference number 158 has been corrected to number 168, in FIG. 10, reference number 230 has been added and in FIG. 11, the words "AND TO RAM" have been removed.

Attachment: Replacement Sheets  
Annotated Sheets Showing Changes



3/7

DATA WRITE OPERATION

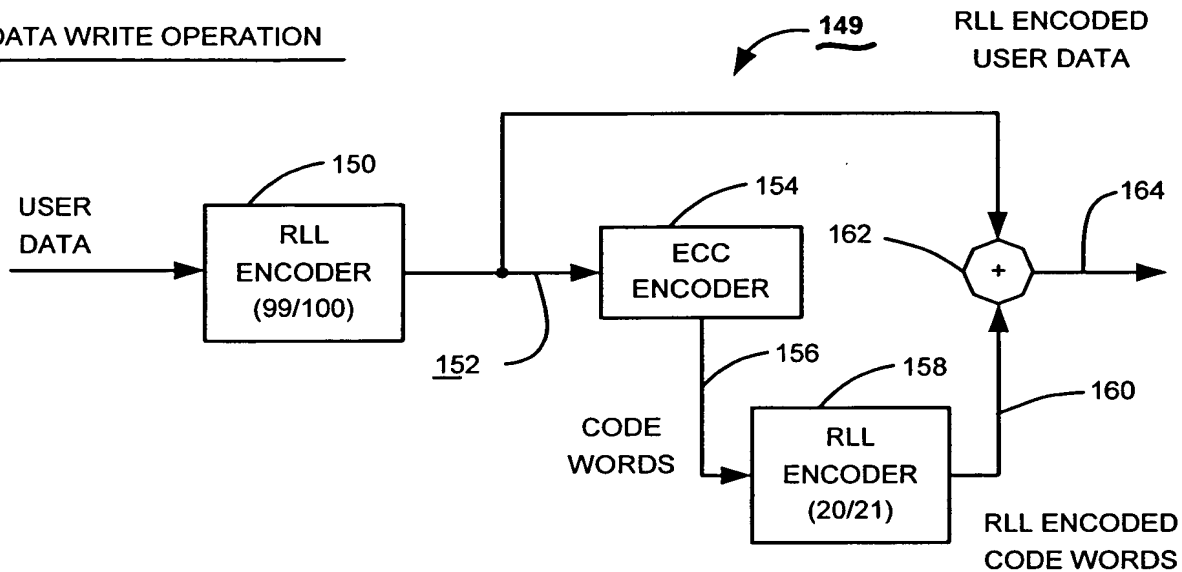


FIG. 6

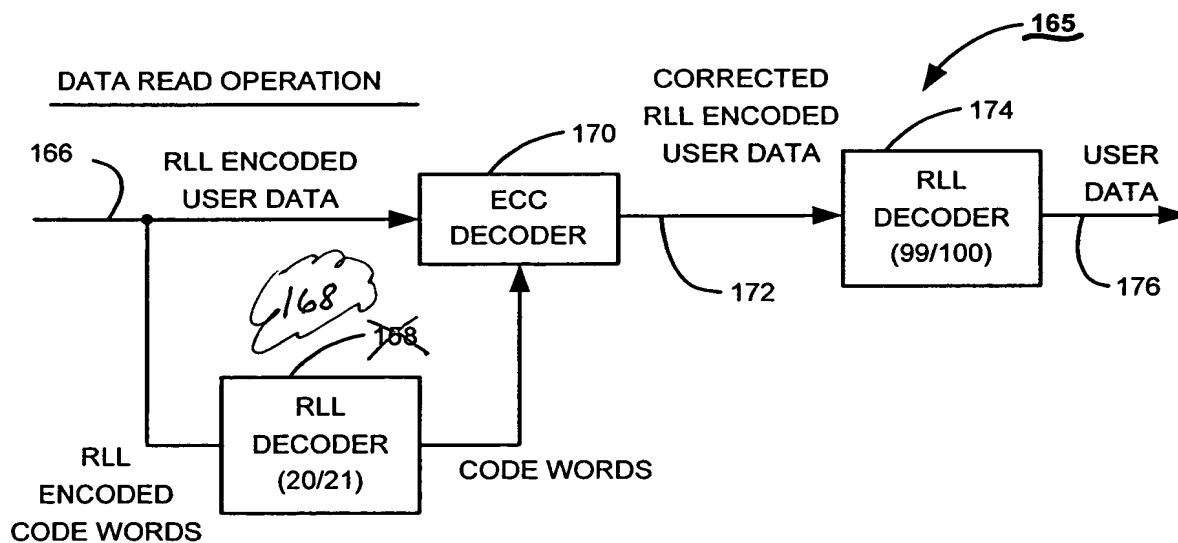


FIG. 7



5/7

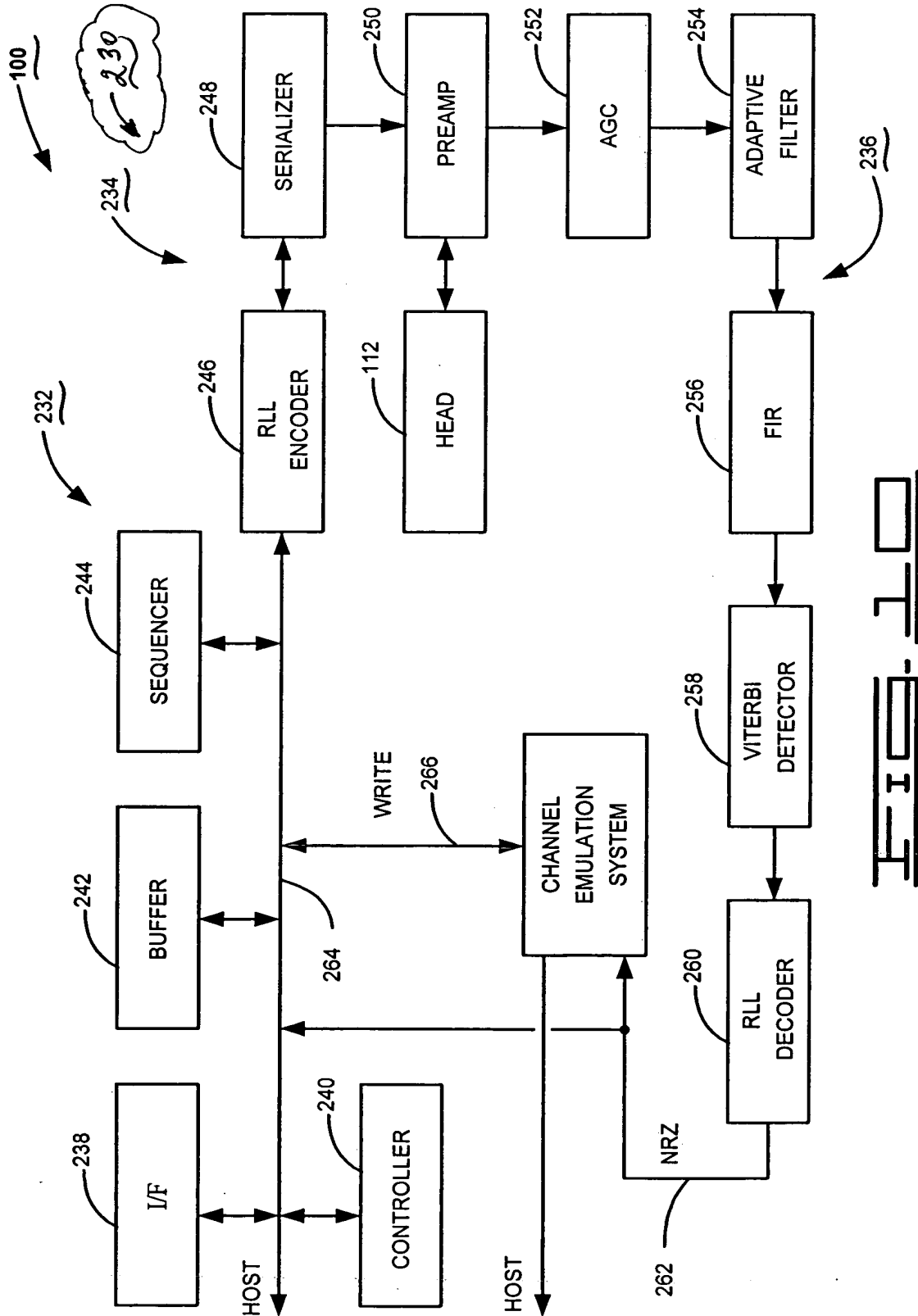


FIG. 10





6/7

